

Application No.: 09/886,776

Docket No.: JCLA6195

AMENDMENTS**In The Claims:**

Please amend the claims as follows.

1. (currently amended) An CMOS image sensor wherein image lag at low light levels is reduced by controlling a reset level, and wherein an amplifier gain setting is used for determining whether to use a hard reset or a soft reset.

2. (previously presented) An improved CMOS image sensor wherein image quality is improved at low light levels without compromising performance at high illumination by using a hard or soft reset dependent on a gain signal level.

3. (currently amended) An image CMOS sensor with reduced image lag comprising:
an imaging device for acquiring image data;
a reset transistor for resetting the image device;
a readout transistor for providing pixel information as an output; and
a selection transistor for selecting between imaging devices, wherein image lag is reduced by controlling a reset level; and
an amplifier gain setting for determining whether to use a hard reset or a soft reset.

Claim 4. (canceled)

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5. (original) The CMOS image sensor of claim 3, wherein the imaging device is a photodiode.

6. (previously presented) The CMOS image sensor of claim 3, wherein all transistors are of same type.

7. (original) The CMOS image sensor of claim 3, wherein the reset level is independent of a preceding signal level.

8. (original) The CMOS image sensor of claim 3, wherein a drain of the reset transistor is connected to a voltage that is less than a supply voltage minus a threshold voltage.

9. (previously presented) The CMOS image sensor of claim 3, wherein a reset drain voltage is switched between a supply voltage and a voltage that is less than the supply voltage minus a threshold voltage.

10. (original) The CMOS image sensor of claim 3, wherein a reset drain level is determined by using gain of one color of pixel.

11. (original) The CMOS image sensor of claim 3, wherein a reset drain level is determined by using a middle gain.

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12. (original) The CMOS image sensor of claim 3, wherein a reset drain level is changed only when gains of all color of pixels satisfy threshold conditions.

13. (currently amended) A CMOS image sensor with reduced image lag comprising:
an imaging device for acquiring image data;
a reset transistor for resetting the image device;
a readout transistor for providing pixel information as an output; and
a selection transistor for selecting between imaging devices, wherein image lag is reduced by controlling a reset level which is switchable between a supply voltage and a supply voltage minus a threshold voltage of the reset transistor; and
an amplifier gain setting for determining whether to use a hard reset or a soft reset.

Claim 14. (canceled)

15. (original) The CMOS image sensor of claim 13, wherein the imaging device is a photodiode.

16. (original) The CMOS image sensor of claim 13, wherein all transistors are of a same type.

17. (original) The CMOS image sensor of claim 13, wherein the reset level is independent of a preceding signal level.

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18. (original) The CMOS image sensor of claim 13, wherein a drain of the reset transistor is connected to a voltage that is less than a supply voltage minus a threshold voltage.

19. (previously presented) The CMOS image sensor of claim 13, wherein a reset drain voltage is switched between a supply voltage and a voltage that is less than the supply voltage minus a threshold voltage.

20. (original) The CMOS image sensor of claim 13, wherein a reset drain level is determined by using gain of one color of pixel.

21. (original) The CMOS image sensor of claim 13, wherein a reset drain level is determined by using a middle gain.

22. (original) The CMOS image sensor of claim 13, wherein a reset drain level is changed only when gains of all color of pixels satisfy threshold conditions.